

WHAT IS CLAIMED IS:

- 1 1. A reconfigurable chip comprising:
2 a despreaders function block including complex multiplier units, the
3 despreaders function block including multiplexers to allow the selection of different
4 operation configurations for the despreaders function block; and
5 interconnect elements operably connected to the despreaders function
6 block the interconnect elements adapted to selectively connect together the
7 despreaders function block with other reconfigurable units.
- 1 2. The reconfigurable chip of Claim 1 wherein the complex
2 multiplier unit comprises a complex half multiplier unit.
- 1 3. The reconfigurable chip of Claim 1 wherein the complex half
2 multiplier unit comprises a 1-bit complex half multiplier unit.
- 1 4. The reconfigurable chip of Claim 3 wherein the 1-bit complex
2 half multiplier is implemented using at least one multiplexer and an inverter.
- 1 5. The reconfigurable chip of Claim 1 wherein the despreaders
2 function box can also implement a correlation function.
- 1 6. The reconfigurable chip of Claim 1 wherein the despreaders
2 function block includes a number of despreaders trees:
- 1 7. The reconfigurable chip of Claim 1 wherein the despreaders trees
2 include a number of complex half multiplier units connected to adder units.

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1 8. The reconfigurable chip of Claim 1 wherein the despreaders
2 function block is controlled by an instruction stored in an associated instruction
3 memory.

1 9. The reconfigurable chip of Claim 1 wherein the despreaders
2 function block includes multiple block input multiplexers and at least one block
3 output multiplexer.

1 10. A reconfigurable chip including:
2 a despreaders function block including complex multiplier units, the
3 despreaders function block including multiplexers to allow the selection of different
4 operation configurations for the despreaders function block; and
5 an instruction memory storing multiple instructions for the despreaders
6 function block

1 11. The reconfigurable chip of Claim 10 wherein the complex
2 multiplier unit comprises a complex half multiplier unit.

1 12. The reconfigurable chip of Claim 11 wherein the complex half
2 multiplier units include at least one multiplexer and an inverter.

1 13. The reconfigurable chip of Claim 10 wherein the despreaders
2 function block can also implement a correlator function.

1 14. The reconfigurable chip of Claim 10 wherein the despreaders
2 function block can also implement a multiplication function.

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1 15. The reconfigurable chip of Claim 10 wherein the despreader
2 function block includes despreader trees.

1 16. The reconfigurable chip of Claim 15 wherein the despreader trees
2 include complex half multiplier units and adders.

1 17. The reconfigurable chip of Claim 10 wherein the despreader
2 function block includes multiple block input multipliers and at least one block
3 output multiplexer.

1 18. The reconfigurable chip of Claim 10 further comprising
2 interconnect elements operably connected to the despreader function block, the
3 interconnect elements adapted to selectively connect the other despreader function
4 block with other reconfigurable units.

1 19. A despreader function block on a reconfigurable chip, the
2 despreader function block including:
3 multiple block input multiplexers;
4 despreader tree units including complex multiplier units, the despreader
5 tree units operably connected to the multiple block input multiplexers; and
6 at least one block output multiplexer operably connected to the selectable
7 despreader tree units.

1 20. The despreader function block of Claim 19 wherein the complex
2 multiplier units comprise complex half multiplier units.

1 21. The despreader function block of Claim 19 wherein the complex
2 half multiplier units comprise a multiplexer and an inverter.

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1 22. The despreader function block of Claim 19 wherein the
2 despreader tree units further include adder elements.

1 23. A reconfigurable chip including the despreader function block of
2 Claim 19.

1 24. The reconfigurable chip of Claim 23 further comprising an
2 interconnect element operably connected to the despreader function block to
3 operably connect together the despreader function block with other reconfigurable
4 units.

1 25. The reconfigurable chip of Claim 23 further comprising an
2 instruction memory showing multiple instructions for the despreader function
3 block.

1 26. The despreader function block of Claim 19 wherein the
2 despreader tree units can also implement correlation functions.

1 27. The despreader function block of Claim 19 wherein the
2 despreader function block can also implement a multiplication function.

1 28. A reconfigurable chip comprising:
2 multiple despreader blocks, the despreader blocks adapted to despread
3 input signals using an PN sequence, the selectable blocks also being selectable to a
4 non-despreader function; and
5 reconfigurable functional units operably connectable to the despreader
6 blocks, the reconfigurable functional units including an arithmetic logic unit.

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1 29. The reconfigurable chip of Claim 28 wherein the despreaders
2 function block include complex half multiplier units.

1 30. The reconfigurable chip of Claim 28 wherein the complex half
2 multiplier units are implemented using multiplexers and an inverter.

1 31. The reconfigurable chip of Claim 28 wherein the despreaders
2 function blocks are implemented using a despreaders tree.

1 32. The reconfigurable chip of Claim 31 wherein the despreaders tree
2 is implemented using a number of complex half multiplier units and adders.

1 33. The reconfigurable chip of Claim 28 wherein the despreaders
2 blocks can also implement a correlator function.

1 34. The reconfigurable chip of Claim 28 wherein the despreaders
2 blocks can also implement a multiplication function.

1 35. The reconfigurable chip of Claim 28 further comprising
2 interconnect elements operably connected to the despreaders function block to
3 interconnect between the reconfigurable functional units and the despreaders blocks.

1 36. The reconfigurable chip of Claim 28 wherein input multiplexers
2 for the despreaders blocks can be selected to connect to operative nearby
3 reconfigurable functional units.

1 37. The reconfigurable chip of Claim 28 wherein the despreaders
2 function block includes multiplexers and at least one block output multiplexer.

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- 1 38. The reconfigurable chip of Claim 28 further comprising an
- 2 instruction memory storing multiple instructions for the despreaders function block.

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